বিদ্যাসাগর বিশ্ববিদ্যালয়

VIDYASAGAR UNIVERSITY

Question Paper

B.Sc. Honours Examinations 2021

(Under CBCS Pattern)

Semester - III

Subject : PHYSICS

Paper : C 7 - T & P

Full Marks : 60 (Theory - 40 + Practical - 20)

Time : 3 Hours

Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.

[DIGITAL SYSTEMS AND APPLICATIONS]

(Theory : Marks - 40)

Group - A

Answer any ***three*** of the following questions : 12×3=36

1. (a) What is Universal gate? Design Ex-OR gate using NOR gate only. 1+2

   (b) Draw a circuit diagram of an AND gate using DTL. Explain its operation. 2+2

   (c) Explain how an OR gate can be converted to AND gate. 3

   (d) Perform the binary subtraction using 2's complement form. (1110011–10011) 2

2. (a) Convert Hexagonal Number $(2F9A)_{16}$ to equivalent Binary Number. 2

(b) Write down the sop expression of the Boolean expression

$$f(A,B,C,D) = \sum_m (1,3,4,6,8,9,11,13,15) + \sum_d (0,2,14)$$ 2

(c) Find the decimal equivalant of 111.1011 2

(d) Find the output of K – Map $\rightarrow$ 2

C \ AB	00	01	11	10
0		1		1
1	1		1	

(e) Design a 1 : 2 DeMuX using NAND GATES. 2

(f) Prove the identity $\overline{AB} + \overline{A} + AB = 1$ 2

(g) What are the volatile and non-volatile Memories in a micro-processor? 2

3. (a) (i) What is Multiplexer? Design 4 to 1 Multiplexer using Basic gates?

(ii) Realize : $Y = \overline{A}\,B + \overline{B}\,\overline{C} + A\,\overline{B}\,C$, using 4 to 1 Multiplexer. 1+2+3

(b) What is full adder? How can it be implemented by logic gates? Draw the logic block diagram for adding two decimal numbers 7 and 12. 1+2+3

4. (a) What is digital comparator? Draw a single bit comparator using basic gates. 1+3

(b) Define register. Constrtuct a 4 bit register using J-K flip-flops. Write down the table for readings of shift register after each clock pulse by assuming the data 1011. 1+3+3

(c) Represent $(2^{11}–1)$ into hexadecimal number system. 1

5. (a) What is synchronous counter? What is its advantage over asynchronous counter? Draw the block diagram of a 3-bit synchronous counter. Explain its operation with its operation with the necessary diagram. 1+2+3+3

(b) Draw the circuit diagram of a 4-bit SISO register using D-type flipflops. 3

6. (a) Draw a Master-Slave JK flip-flop system using universal gates. Explain its operation. What are the functions of preset and clear inputs? What is meant by race around condition? How can it be avoided? 2+3+3+1+1

(b) What do you mean by edge triggering in flip-flop? 2

Group - B

Answer any ***two*** of the following questions : 2×2=4

7. An equality detector gives an output 1 if A and B are both 1 or if A and B are both zero. Implement the circuit.

8. In a D/A converter the full-scale output voltage is 5V. Find its resolution.

9. How many address lines are required to address two megabytes (2048K) of memory?

10. A negative logic OR is equivalent to positive logic AND. Explain.

(Practical : Marks - 20)

Group - A

Answer any ***one*** of the following questions : 20×1=20

1. Design an astable multivibrator of frequency of 10 KH_Z with 2/3 rd duty cycle using 555 timer IC.

(a) Theory

(b) Implementation of the circuit and recording of data.

(c) Results and discussion. 8+8+4

2. Design a 4-bit shift register PISO using D type JK - F-F ICS.

(a) Theory

(b) Implementation of the circuit and recording of data.

(c) Results and discussions. 8+8+4

3. Design a R-S flip-flop using NAND gates.

(a) Theory

(b) Implementation of the circuit and recording of data.

(c) Results and discussion. 8+8+4

4. Design a 4-bit binary adder and check the result for the set of data.

(a) Theory

(b) Implementation of the circuit and recording of data.

(c) Result and discussion. 7+10+3

5. Design AND, OR, EX-OR gates using IC–7400 and verify their truth tables.

(a) Theory

(b) Implementation of the circuits and taking data.

(c) Result and discussion. 7+10+3