Physics(Hons.)

Semester-IV

CC-10

Biasing of a transistor

Dr. Bidyut Samanta

Online-5 (BJT-3)

A transistor is found to act most linearly when its operation is confined to the active region. So a transistor must be operated in the active region to achieve undistorted amplification.

.Biasing of a transistor means not only the forward biasing of the emitter-base junction and reverse biasing the collector base junction but also the establishment of the d.c. operating point at suitable location in the active region of the characteristics. An operating point means a point on the characteristic curves, whose coordinates give the d.c. current flowing through the transistor and the d.c. voltage actually acting across it. It can be done by connecting the transistor to external sources via suitable circuits. The d.c. operating point is also known as quiescent operating point or simply Q-point.

When an input signal is applied the total instantaneous values of current and voltage vary about the d.c. values. The output a.c. power (voltage or current) is usually greater than the a,c, power (voltage or current). This extra energy comes from the applied d.c. sources

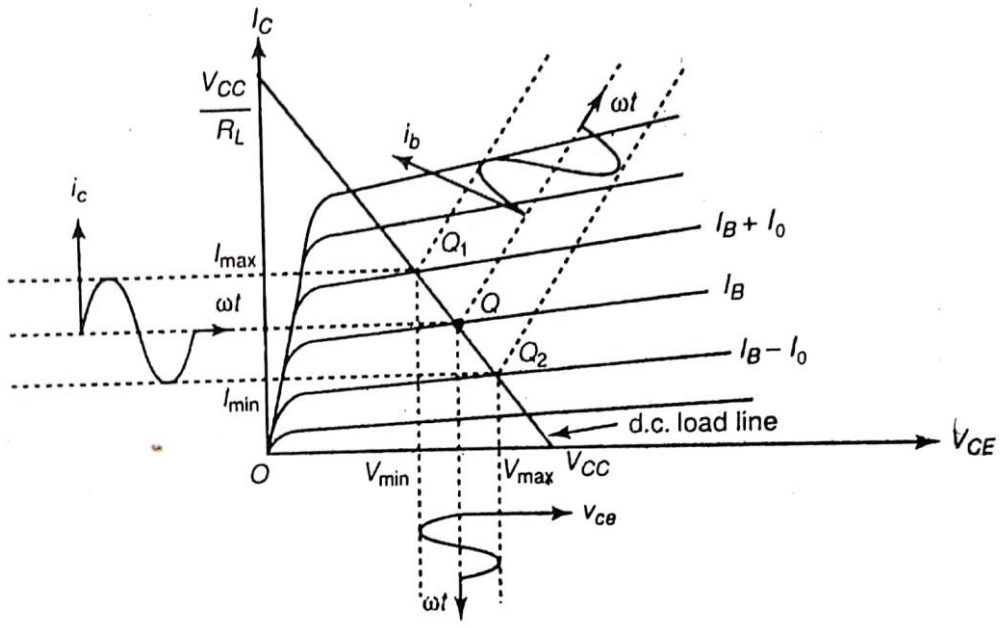

Fig.1 CE amplifier input-output signal variations

To select the position of Q-point one has to consider the following points:

(i) The amplitude of the signal
(ii) The load of the amplifier
(iii) The available d.c. power
(iv) Allowable distortion, etc.

The operating point is to be so chosen that the distortion, power dissipation, variation of transistor parameters with the operating point are minimum and economy of power supply is optimum. For large signal amplifiers the Q-point is to be so located that maximum output power is obtained with maximum efficiency and minimum distortion.

Very often Q-point is chosen at the middle of the active region such that during the swing of input signal, the transistor is neither driven to cut-off nor to saturation. Another point is that various transistor ratings must not be exceeded. Some of these limits are maximum collector voltage, maximum collector current and maximum collector dissipation, $P_{C,max}$. The Q point must be well below the maximum collector dissipation hyperbola given by $V_{CE}.I_C = P_{c,max} = constant$

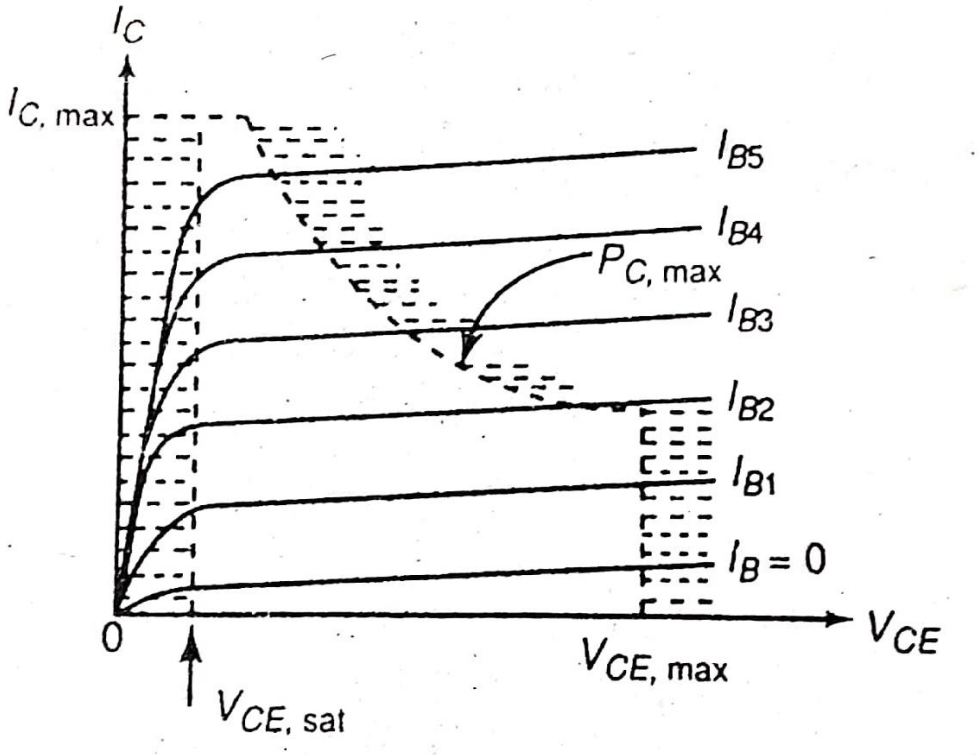

Fig.2 The limits of operation of a transistor in CE mode.

Stability of Biasing

Since transistor is a semiconductor device its properties are sensitive to the variation in temperature. Unless the bias arrangement is correctly designed the variations of transistor parameters may shift the Q-point and hence the desired operation. So the biasing arrangement should have the ability to counteract the shift of operating point due to temperature and other causes.

The stability of biasing means the ability of a biasing arrangement to counteract any drift of Q-point.

The collector current, I_C changes with temperature due to temperature dependence of I_{CO} and β and V_{BE}. I_{CO} almost doubles for every 10°C rise in temperature; β increases with temperature; V_{BE} decreases at the rate few mV/°C. Also they are likely to be significantly different for two transistors having same specification. Sometimes we need to replace a transistor by another of same type. So the biasing arrangement should have the ability to reduce the effect of all such changes in transistor parameters.

I_{CO} is the quantity which varies most with temperature. So the differential coefficient $S = \frac{\partial I_C}{\partial I_{CO}}$ with β and V_{BE} constants can be taken as the measure of temperature stability of Q-point. Smaller is the value of S, better is the stability.

If the biasing arrangement fails to achieve thermal stabilization then an increase in temperature increases I_{CO} and hence I_C. This heats the collector junction more and increases I_{CO}. The process is thus cumulative in nature and may cause the junction temperature to exceed its rated value. Thus the device may burn out. This phenomenon is known as thermal-runaway.

The variation of I_C due to variation of β is expressed by another stability factor: $S_\beta = \frac{\partial I_C}{\partial \beta}$ where I_{CO} and V_{BE} are considered constant. The variation of I_C with V_{BE} is expressed by the stability factor: $S_V = \frac{\partial I_C}{\partial V_{BE}}$ where both I_{CO} and β remain constant.

A good biasing arrangement is one that can stabilize the Q-point so that the amplifier can be used in a changing temperature environment.

Fixed Bias Arrangement

Consider an n-p-n transistor with fixed bias in CE mode as shown in Fig.1.

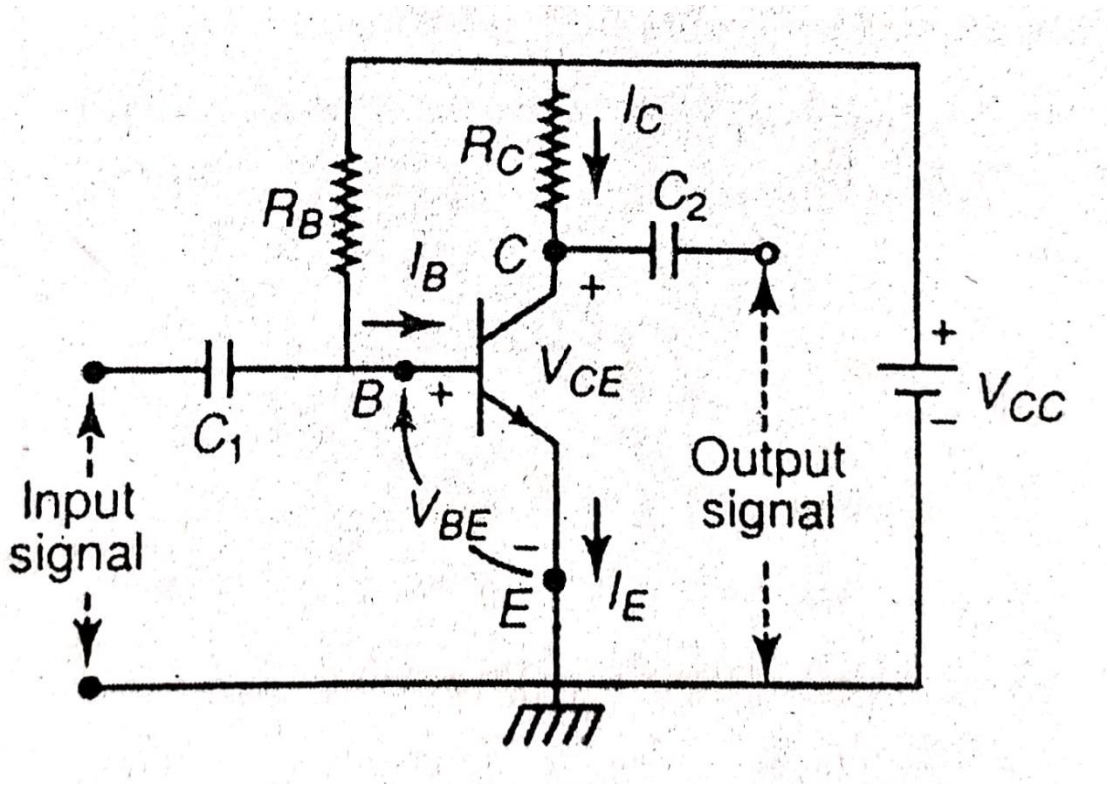

Fig. 3 Fixed Biasing of an n-p-n transistor in CE mode

C_1 and C_2 are the coupling capacitors, Their reactance are chosen very small at the lowest signal frequency so that they practically offer short circuited path to a.c. but for d.c. they act as open circuit. These capacitors make it possible to couple the input signal source to the amplifier or the output of the amplifier to the input of another amplifier without disturbing its d.c. bias.

The single d.c. source V_{CC} is used to make the emitter junction forward biased and the collector junction reverse biased.

R_B is called base bias resistance and R_C is the load resistance.

Determination of Q-point using load line

Applying KVL around base-emitter circuit loop we get

$$V_{CC} = I_B R_B + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad (1)$$

Usually $V_{CC} \gg V_{BE}$ and hence,

$$I_B \approx \frac{V_{CC}}{R_B} \qquad (2)$$

Thus any change in V_{BE} due to change in temperature will have practically no effect on I_B.

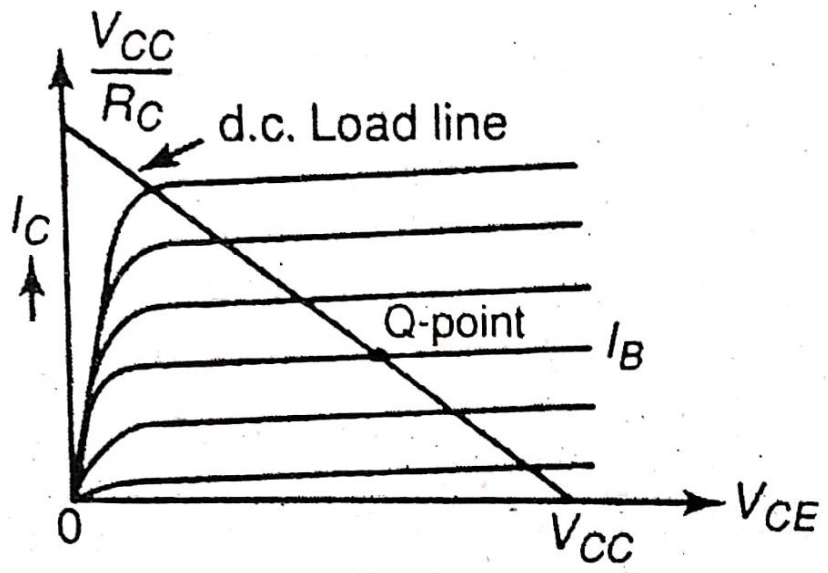

Fig.4 Q-point of a fixed bias circuit

Since the base bias current I_B is constant, the circuit is called fixed bias circuit. Applying KVL around the collector circuit we get

$$V_{CC} = I_C R_C + V_{CE}$$

It represents a straight line in the $V_{CE} - I_C$ plane. It is called d.c. load line. To find the Q-point a load line is plotted on the output characteristic curves as a line connecting the points $\left(0, \frac{V_{CC}}{R_C}\right)$ *and* $(V_{CC}, 0)$.

The coordinates of the point of intersection of the load line and characteristic curve corresponding to the fixed value of I_B as given by equation (2) gives the actual d.c. value of collector current and the the d.c. value of V_{CE} actually operating across the transistor. This point is the Q-point.

The circuit parameters are to be chosen properly such that the Q-point lies at the middle of the load line and not near the cut-off or saturation .

Analytical determination of Q-point

If transistor characteristics are not available but β is known then the Q-point may be determined analytically. We know:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad (1)$$

$$I_C = \beta I_B + (1 + \beta) I_{CO} \qquad (2)$$

$$V_{CE} = I_C R_C - V_{CC} \qquad (3)$$

Stability factors:

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B} + (1 + \beta) I_{CO} \quad (4)$$

$$\therefore S = \frac{\partial I_C}{\partial I_{CO}} = (1 + \beta) \quad (5)$$

$$S_\beta = \frac{\partial I_C}{\partial \beta} = \frac{V_{CC} - V_{BE}}{R_B} + I_{CO} \quad (6)$$

$$S_V = \frac{\partial I_C}{\partial V_{BE}} = -\frac{\beta}{R_B} \quad (7)$$

We see from equation(5) that the collector current changes $(1 + \beta)$ times the change in I_{CO} due to temperature. Since, $\beta \gg 1$, the circuit cannot achieve stability of Q-point against temperature.

Equation (4) indicates that any change in β directly affects I_C. So the circuit cannot also achieve stability against changes in β.

However, because of simplicity and low cost the fixed bias circuit is used in many cases.

Equation (6) & (7) show that stability of Q-point against variations in β and V_{BE} can be improved by choosing a large R_B.