

MICROPROCESSOR

BCA 3RD SEMESTER 2020

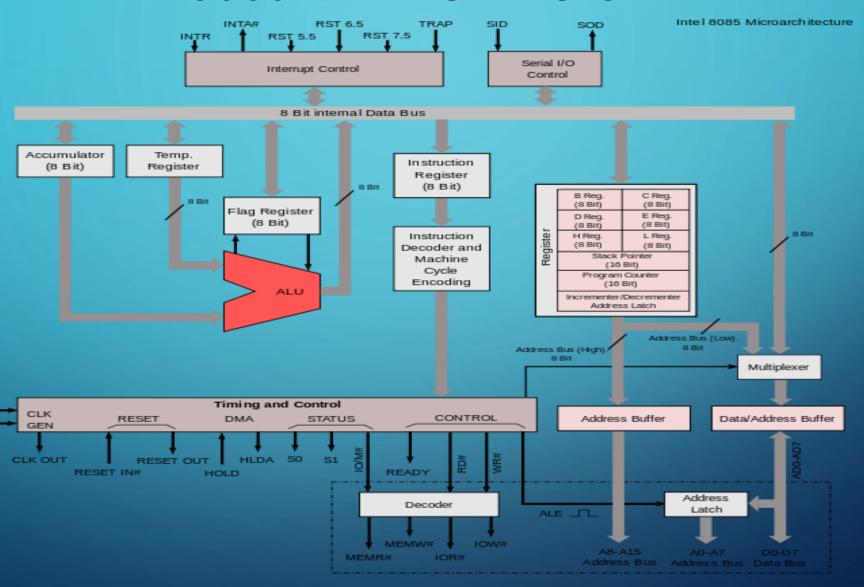
LECTURE-3

SUBHADIP MUKHERJEE

DEPARTMENT OF COMPUTER SCIENCE

KHARAGPUR COLLEGE

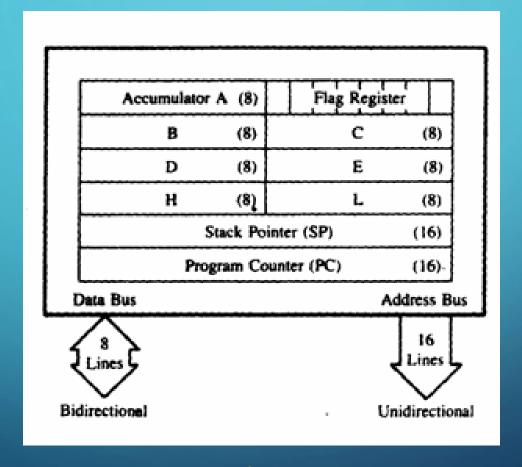
8085 MP ARCHITECTURE



8085 MP ARCHITECTURE (CONT.)

- Control Unit
- Arithmetic Logic Unit

PROGRAMMING MODEL OF 8085 MP



PROGRAMMING MODEL OF 8085 MP (CONT.)

REGISTERS

Program Counter (PC)

The function of the program counter is to point to the memory address from which the next byte is to be fetched.

Stack Pointer (SP)

It points to a memory location in R/W memory, called the stack.

Accumulator

PROGRAMMING MODEL OF 8085 MP (CONT.)

Flag Registers

Zero(Z)

Carry (CY)

Sign (S)

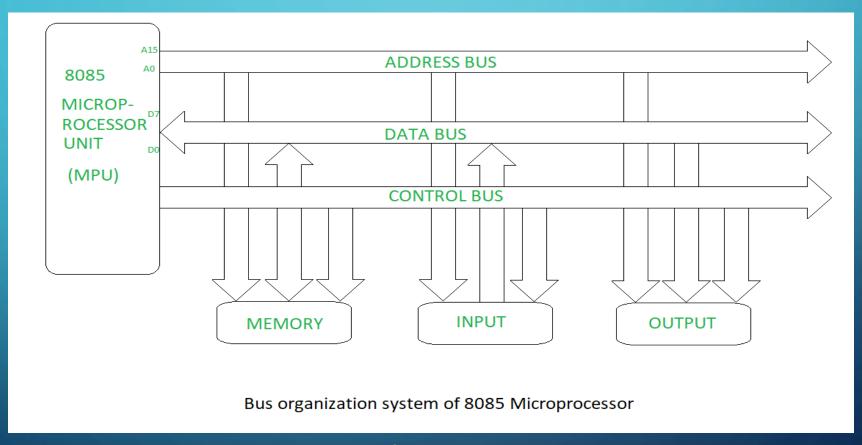
Parity (P)

Auxiliary Carry (AC)

Other Special Registers

- Instruction Register / Decoder
- Memory Address Register (MAR)
- Control Generator
- Register Selector

The Bus System



The Bus System (Cont.)

1. Address Bus

The address bus is a group of 16 lines

The address bus is unidirectional

The 8085 with its 16 lines is capable of addressing 64 K memory locations.

2. Data Bus

The data bus is a group of eight lines used for dataflow

They are bidirectional

The Bus System (Cont.)

1. Control Bus

The control bus consists of various single lines that carry synchronization signals.

These signals are used to identify a device type which the processor intends to communicate.

THANK YOU

End of Lecture- 3